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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/258,961	03/01/99	JIANG T	98-0645.1

MMC1/0321

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EXAMINER	
PAREKH,N	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 03/21/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/258,961	Jiang et al
Examiner	**Group Art Unit**
Nitin Parekh	2811

☒ Responsive to communication(s) filed on *Jan 16, 1901*

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claim

☒ Claim(s) *24-36* is/are pending in the applicat

Of the above, claim(s) _____ is/are withdrawn from consideration

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *24-36* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☒ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). *2 and 6*

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 24-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art (APA) in view of Lee et al (US Pat. 5796586) and/or Akram et al (US Pat. 5739585). Regarding claims 24 and 25, the admitted prior art (Fig.1A and B; pages 2-4) et al discloses a semiconductor package comprising :

- a substrate comprising a first surface, a second surface, a plurality of conductors and ball bonding pads formed on the first surface and a bonding opening from the first surface to the second surface

- a semiconductor die having a first outline and a face on the bonding opening bonded to the second surface

- first mask on the first surface of the substrate comprising a plurality of via openings aligned with the ball bonding pads

- a second mask substantially covering a second surface of the substrate

- an adhesive layer between the die and the substrate in the die attach area to bond the face to the second mask and the substrate,

- a plurality of wires placed through the bonding opening and wire bonded to the die and to the conductors

- an encapsulating material encapsulating the die and the second mask, and

- a glob top in the bonding opening encapsulating the wires.

The admitted prior art fails to specify directly bonding the die to the second surface and having an opening in the second mask including a second outline substantially matching the first outline. Lee et al teach using a second mask having an opening through the mask with a second outline (see hatched mask area 218' with a second outline- Fig. 7; Col. 7, line 55) substantially matching that of the first outline with an open die attach area (see first outline area 204- Fig. 7) on the second surface so that the die is directly bonded to the second surface so that the solder mask can provide a better resistance against cracking at the substrate surface (Fig. 7 and Fig. 1-6; Col. 1-8). Furthermore, Lee et al disclose die attach area, conventionally, not being covered with solder mask so that the die attaches directly to the substrate surface (Col. 8, line 7). Akram et al teach using conventional die attach technique where the die (18 in Fig. 10; Col. 9, line 24) is face-bonded to the second surface using typical adhesive/fill materials (Col. 4, line 26) such as an epoxy, silicone, polyimide, other dielectric material, etc. Therefore, it would have been obvious to the person of ordinary skill in the art at the time invention was made to use a second mask having an opening and a second outline substantially matching the first outline so that the die is bonded directly to the second surface to prevent the cracking of the solder mask using Lee et al and Akram et als teachings in the admitted prior art as cited in claims 24 and 25.

Claim 26 is rejected as explained above for claims 24.

The combined teachings of Lee et al and/or Akram et al apply to claims 27-29 as explained above for claim 24-26.

The combined teachings of Lee et al and/or Akram et al apply to claims 30-33 as explained above for claims 24-26.

The combined teachings of Lee et al and/or Akram et al apply to claims 34-36 as explained above for claims 24-26.

Response to Arguments

3. Applicant's arguments filed on 01-16-01 have been fully considered but they are not persuasive.

A. Applicant contends that Lee et al's solder mask is configured to protect the circuit traces. However, Lee et al further teach that the solder mask provides better resistance to cracking than typical adhesives (Col. 7, line 60) on any surface on the substrate. Furthermore, Lee et al disclose that conventionally the die attach area is not covered by the solder mask. Therefore, Lee et al's

teaching related to the solder mask layout is applied to the APA to improve the cracking resistance.

B. Applicant contends that in Lee et al's layout the die attach area must leave room for wire bonding/tips. However, it is conventional in chip packaging art to define the desired area/outline for the solder mask using photo processing to achieve any desired area with the solder mask outside the die attach outline in APA or Akram et al's package.

C. Applicant contends that APA in view of Lee et al do not teach using filled epoxy/adhesive. However, Akram et al teach using conventional die attach adhesive/fill materials such as an epoxy, silicone, polyimide, other dielectric material, etc (Col. 4, line 26).

Papers related to this application may be submitted directly to Art Unit 2811 by facsimile transmission. Papers should be faxed to Art Unit via Technology Center 2800 fax center located in Crystal Plaza 4, room 4C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number in (703) 305-3410. The examiner can be normally reached on Monday-Friday from 08:30 am-5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (703) 308-2772. The fax number for the organization where this application or proceeding is assigned is (703) 308-7722 or 7724.

Nitin Parekh

03-15-01

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER